1M X 9 DRAM SIMM Memory Module

FEATURES

- Performance range:

	t_{RAC}	t_{CAC}	t_{RC}
STI91000A-60	60ns	15ns	110ns
STI91000A-70	70ns	20ns	130ns
STI91000A-80	80ns	20ns	150ns

- Fast Page Mode operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- TTL compatible inputs and outputs
- Single +5V ± 10% power supply
- 1024 cycles/16ms refresh
- JEDEC standard pinout
- Available in tin or gold edge connectors

PIN NAMES

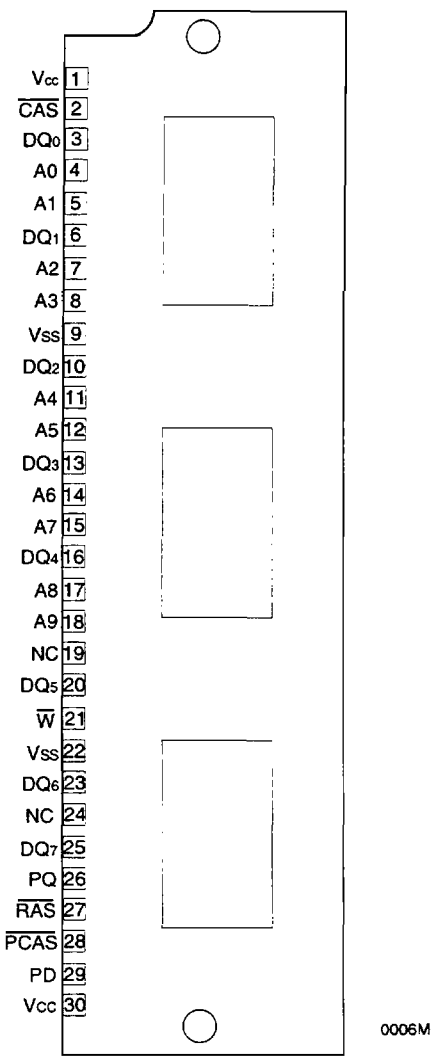
Pin Name	Pin Function
A_0-A_9	Address Inputs
DQ_0-DQ_7	Data In/Out
PD	Data In for Parity
PQ	Data Out for Parity
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Adress Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{PCAS}$	$\overline{CAS}$ for Parity
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

GENERAL DESCRIPTION

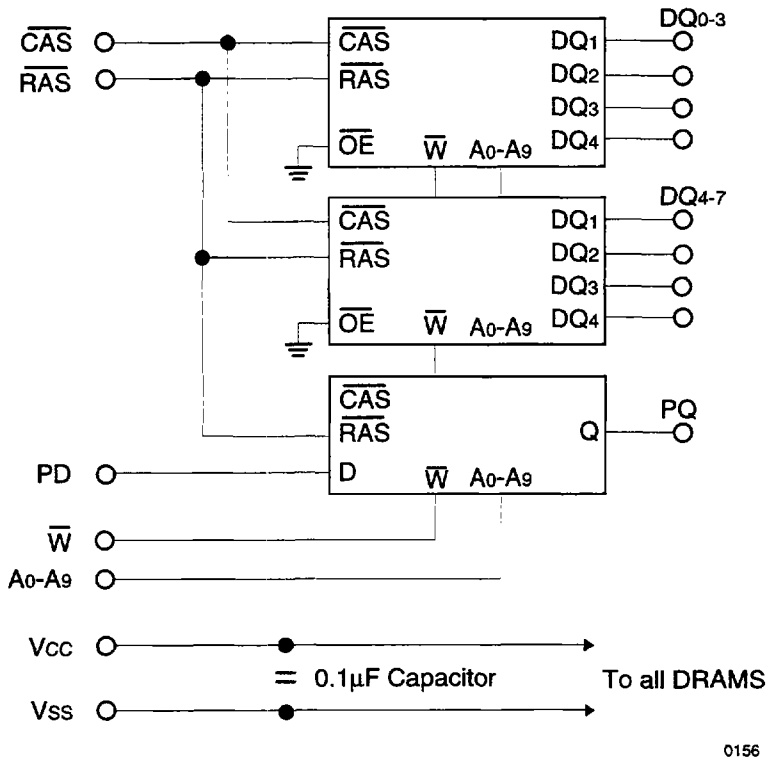
The Simple Technology STI91000A is a 1M bit x 9 Dynamic RAM high density memory module. The Simple Technology STI91000A consist of two CMOS 1M x 4 DRAMs in 20-pin SOJ package and one CMOS 1M x 1 DRAM in 20-pin SOJ package mounted on a 30-pin glass epoxy substrate. A 0.1µF decoupling capacitor is mounted for each DRAM.

The STI91000A is a Single In-line Memory Module with tin (STI91000A-xxT) or gold (STI91000A-xxG) edge connections and is intended for mounting into 30-pin edge connector sockets.

PIN CONFIGURATION (Front View)



FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-1 to +7.0	V
Storage Temperature	T_{stg}	-55 to +150	°C
Power Dissipation	P_D	1.8	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the oprerational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	-1.0	—	0.8	V

DC AND OPERATION CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @t_{RC}=min.)	STI91000A-60	I_{CC1}	—	220	mA
	STI91000A-70		—	195	mA
	STI91000A-80		—	170	mA
Standby Current ($\overline{RAS}$, $\overline{CAS}$=V_{IH})		I_{CC2}	—	6	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$, Address Cycling @t_{RC}=min.)	STI91000A-60	I_{CC3}	—	220	mA
	STI91000A-70		—	195	mA
	STI91000A-80		—	170	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @t_{PC}=min.)	STI91000A-60	I_{CC4}	—	165	mA
	STI91000A-70		—	140	mA
	STI91000A-80		—	115	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)		I_{CC5}	—	3	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	STI91000A-60	I_{CC6}	—	220	mA
	STI91000A-70		—	195	mA
	STI91000A-80		—	170	mA
Input Leakage Current (Any input 0≤V_{IN}≤6.5V, all other pins not under test=0V)		I_{IL}	-30	30	µA
Output Leakage Current (Data out is disabled, 0≤V_{OUT}≤5.5V)		I_{OL}	-10	10	µA
Output High Voltage Level (I_{OH}=-5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	—	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC6} are dependent on output loading and cycling rates. Specified values are obtained with the output open. I_{CC} is specified as an average current.

CAPACITANCE (T_A=25 °C)

Item	Symbol	Min	Max	Units
Input Capacitance (A_0-A_9)	C_{IN1}	—	55	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, W)	C_{IN2}	—	65	pF
Input/Output Capacitance (PD, $\overline{PCAS}$)	C_{IN3}	—	10	pF
Input Capacitance (DQ_0-DQ_7)	C_{DQ}	—	15	pF
Output Capacitance (PQ)	C_Q	—	10	pF

AC CHARACTERISTICS (0 °C≤T_A≤70 °C, V_{CC}=5.0V±10%, See notes 1, 2)

Parameter	Symbol	STI91000A-60		STI91000A-70		STI91000A-80		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3, 4
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	3, 4, 5
Access time from column address	t_{AA}		30		35		40	ns	3, 11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		15		ns	
Column address hold referenced to $\overline{RAS}$	t_{AR}	50		55		60		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	10		15		15		ns	
Write command hold referenced to $\overline{RAS}$	t_{WCR}	45		55		60		ns	6
Write command pulse width	t_{WP}	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		20		20		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10
Data-in hold time	t_{DH}	15		15		15		ns	10
Data-in hold referenced to $\overline{RAS}$	t_{DHR}	50		55		60		ns	6

(continued on the next page)

AC CHARACTERISTICS (continued)

Parameter	Symbol	STI91000A-60		STI91000A-70		STI91000A-80		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Refresh period	t_{REF}		16		16		16	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ set-up time (C-B-R refresh)	t_{CSR}	5		5		5		ns	
$\overline{CAS}$ hold time (C-B-R refresh)	t_{CHR}	15		15		15		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	5		5		5		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40		45	ns	3
Fast Page mode cycle time	t_{PC}	40		45		50		ns	
$\overline{CAS}$ precharge time (fast page)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ pulse width (fast page)	t_{RASP}	60	100,000	70	100,000	80	100,000	ns	
$\overline{W}$ to $\overline{RAS}$ precharge time (C-B-R refresh)	t_{WRP}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time (C-B-R refresh)	t_{WRH}	10		10		10		ns	
$\overline{CAS}$ precharge time (C-B-R counter test)	t_{CPT}	20		25		30		ns	

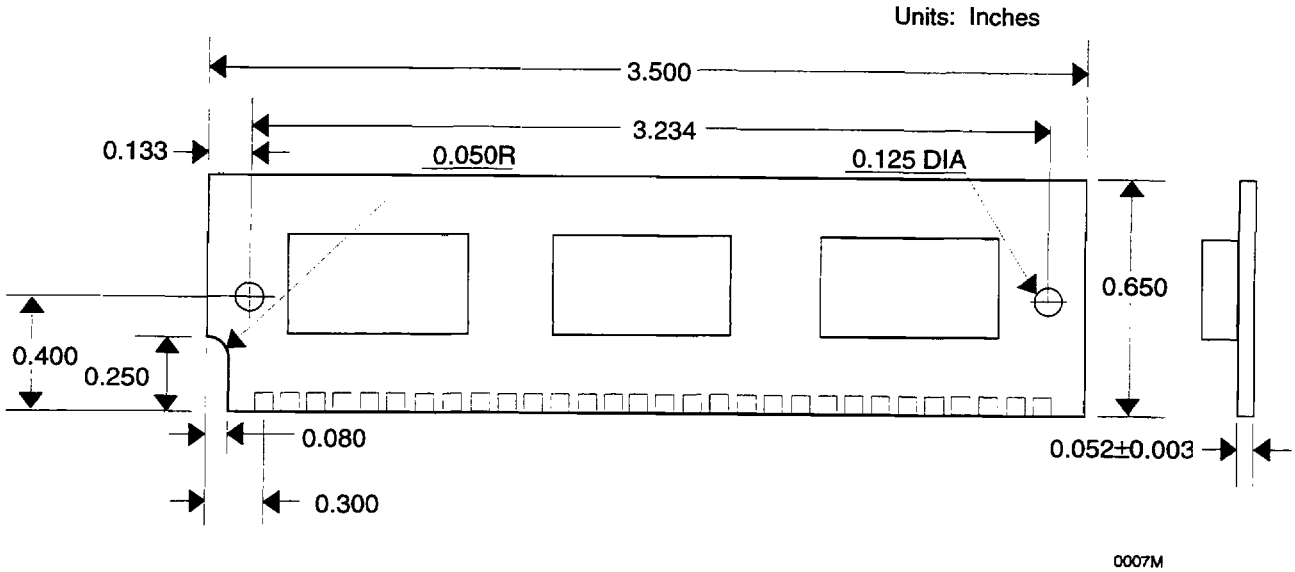
NOTES

1. An initial pause of 200 µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$, and are assumed to be 5ns for all inputs.
3. Measure with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$.
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are non-restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit then access time is controlled by t_{AA}.

TIMING DIAGRAMS

Please refer to attached Timing Chart I.

PACKAGE DIMENSIONS



TOLERANCES: ±0.005 UNLESS OTHERWISE SPECIFIED